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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech I Year II Semester Supplementary Examinations February-2022

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours

Max. Marks: 60

PART-A

(Answer all the Questions 5 x 2 = 10 Marks)

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|---|---|----|
| 1 | a Define duality property. | 2M |
| | b State De Morgan's theorem | 2M |
| | c Explain the applications of Multiplexer | 2M |
| | d Define Race Around Condition | 2M |
| | e Define the Static RAM and Dynamic RAM | 2M |

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

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|---|---|----|
| 2 | a Represent the decimal number 3452 in i)BCD ii)Excess-3 | 5M |
| | b Subtract $(111001)_2$ from (101011) using 1's complement? | 5M |

OR

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|---|--|----|
| 3 | a Design the circuit by Using NAND gates $F = ABC' + DE + AB'D'$ | 5M |
| | b Explain binary to Gray & Gray to binary conversion with example. | 5M |

UNIT-II

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| 4 | Simplify the Boolean expression using K-MAP
$F(A,B,C,D,E) = \sum m(0,1,4,5,16,17,21,25,29)$ | 10M |
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OR

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| 5 | Obtain the a) SOP b) POS expression for the function given below
$F(A,B,C,D) = \sum m(0,1,2,5,8,9,10)$ | 10M |
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UNIT-III

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| 6 | Explain The Half adder. Implement the full adder using two half adders. | 10M |
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OR

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| 7 | a Explain about 2-bit Magnitude Comparator. | 6M |
| | b What is memory decoding? Explain about the construction of 4 X 4 RAM. | 4M |

UNIT-IV

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| 8 | Explain the design of a 4-bit binary counter with parallel load in detail. | 10M |
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| 9 | a What is state assignment? Explain with a suitable example. | 5M |
| | b Explain about Shift Registers. | 5M |

UNIT-V

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| 10 | Design PAL for a combinational circuit that squares a 3-bit number. | 10M |
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OR

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| 11 | a Write difference between PROM, PLA & PAL. | 5M |
| | b Explain about Hamming code. | 5M |

END